We claim:

1. A method for applying test patterns to scan chains in a circuit-under-test, the method comprising:

providing a compressed test pattern of bits;

decompressing the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided; and

applying the decompressed test pattern to scan chains of the circuit-under-test.

2. The method of claim 1 including applying the decompressed test pattern to scan chains of the circuit-under-test as the compressed test pattern is being provided.

3. The method of claim 1 including providing the compressed test pattern through input channels to a circuit-under-test, the number of input channels being fewer than the number of scan chains to which the decompressed pattern is applied.

4. The method of claim 1 wherein providing the compressed test pattern, decompressing the compressed test pattern, and applying the decompressed pattern are performed synchronously at a same clock rate.

5. The method of claim 1 wherein the compressed test pattern is provided at a lower clock rate and the compressed test pattern is decompressed and applied synchronously at a higher clock rate.

6. The method of claim 1 wherein the compressed pattern is provided and decompressed at a higher clock rate and the decompressed pattern is applied synchronously at a lower clock rate.

7. The method of claim 1 wherein decompressing the compressed test pattern comprises generating during a time period a greater number of decompressed test pattern bits than the number of compressed test pattern bits provided during the same time period.

8. The method of claim 7 wherein the greater number of bits is generated by providing a greater number of outputs for decompressed test pattern bits than the number of inputs to which the compressed test pattern bits are provided.

9. The method of claim 7 wherein the greater number of bits is generated by generating the decompressed test pattern bits at a higher clock rate than the clock rate at which the compressed test pattern bits are provided.

10. The method of claim 1 wherein applying the decompressed test pattern to the scan chains comprises applying during a time period a greater number of decompressed test pattern bits to the scan chains than the number of compressed test pattern bits provided during the same time period.

11. The method of claim 1 wherein providing a compressed test pattern comprises generating a serial stream of bits at a tester and applying the serial stream to an input channel of a decompressor coupled to the circuit-under-test.

12. The method of claim 1 wherein providing a compressed test pattern comprises generating a parallel stream of bits at a tester, converting the parallel stream to a serial stream, and applying the serial stream to an input channel of a decompressor coupled to the circuit-under-test.

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13. The method of claim 1 wherein decompressing the compressed test pattern comprises generating each bit of the decompressed pattern by logically combining two or more bits of the compressed test pattern.

14. The method of claim 13 wherein logically combining two or more bits of the compressed test pattern comprises combining the bits with an XOR operation.

15. The method of claim 13 wherein logically combining two or more bits of the compressed test pattern comprises combining the bits with an XNOR operation.

16. The method of claim 1 wherein the compressed test pattern is a deterministic test pattern.

17. The method of claim 1 wherein the providing and decompressing occur within the circuit-under-test.

18. The method of claim 1 wherein the providing and decompressing occur within a tester, the tester applying the decompressed test pattern to scan chains of the circuit-under-test.

19. A system for applying test patterns to scan chains in a circuit-under-test, the method comprising:

means for providing a compressed test pattern of bits;

means for decompressing the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided; and

means for applying the decompressed test pattern to the scan chains of the circuit-under-test.

20. The system of claim 19 wherein the means for decompressing the compressed test pattern into a decompressed test pattern of bits is contained with a tester.

21. The system of claim 19 wherein the means for decompressing the compressed test pattern into a decompressed test pattern of bits is contained with the circuit-under-test.

22. A circuit comprising:

a decompressor adapted to receive a compressed test pattern of bits and decompress the test pattern into a decompressed test pattern of bits as the compressed test pattern is being received;

circuit logic; and

scan chains for testing the circuit logic, the scan chains coupled to the decompressor and adapted to receive the decompressed test pattern.

23. The circuit of claim 22 wherein the decompressor comprises a linear finite state machine adapted to receive the compressed test pattern.

24. The circuit of claim 23 wherein the linear finite state machine comprises a linear feedback shift register.

25. The circuit of claim 23 wherein the linear finite state machine comprises a cellular automaton.

26. The circuit of claim 23 wherein the decompressor includes a phase shifter coupled between the linear finite state machine and the scan chains.

27. The circuit of claim 26 wherein the phase shifter comprises an array of XOR gates.

28. The circuit of claim 26 wherein the phase shifter comprises an array of XNOR gates.

29. The circuit of claim 22 wherein the scan chains are adapted to receive the decompressed test pattern as the compressed test pattern is being received by the decompressor.

30. A circuit comprising:

a decompressor adapted to receive a compressed test pattern of bits and decompress the test pattern into a decompressed test pattern of bits, the decompressor having a plurality of input channels and a plurality of outputs, the input channels receiving in parallel the bits of the compressed test pattern;

circuit logic; and

scan chains for testing the circuit logic, the scan chains coupled to the outputs of the decompressor and adapted to receive the decompressed test pattern in parallel.

31. The circuit of claim 30 including one or more spatial compactors adapted to compress a test response read from the scan chains.

32. A circuit comprising:

a linear finite state machine having input logic gates adapted to logically combine bits stored within the machine with bits received from a compressed test pattern, the state machine generating therefrom a series of bits;

a phase shifter coupled to the linear finite state machine, the phase shifter adapted to logically combine two or more bits generated by the linear finite state machine to produce a decompressed pattern of bits; and

scan chains coupled to the phase shifter and adapted to receive therefrom the decompressed test pattern.

33. The circuit of claim 32 wherein the number of scan chains is greater than the number of input channels.

34. A tester comprising:

storage adapted to store a set of compressed test patterns of bits;

a decompressor coupled to the storage, the decompressor adapted to receive a compressed test pattern of bits provided from the storage and to decompress the test pattern into a decompressed test pattern of bits as the compressed test pattern is being received; and

one or more tester channels coupled to the decompressor, the channels adapted to receive a decompressed test pattern and apply the decompressed test pattern to a circuit-under-test.

35. The tester of claim 34 including a compactor adapted to compact a test response to the decompressed test pattern received from the circuit-under-test.

36. A method for applying test patterns to scan chains in a circuit-under-test, the method comprising:

providing within a tester a compressed test pattern of bits;

decompressing within the tester the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided; and

applying the decompressed test pattern from the tester to scan chains of the circuit-under-test.

37. The method of claim 36 including compacting within the tester a test response to the decompressed test pattern received from the circuit-under-test.

38. A method for applying test patterns to scan chains in a circuit-under-test, the method comprising the following steps:

a step for providing a compressed test pattern of bits;

a step for decompressing the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided; and

a step for applying the decompressed test pattern to scan chains of the circuit-under-test.